UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,505	07/22/2003	Terry Borer	015114-065900US	8087

			EXAMINER
26059	7590	05/19/2006	DOAN, NGHIA M

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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/625,505	BORER ET AL.
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03/09/2006</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,11,16,20-23,25,27,28,30-32 and 34-40* is/are pending in the application.

    4a) Of the above claim(s) *2, 9-10, 12-15, 17-19, 24, 26, 29, and 33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,11,16,20-23,25,27,28,30-32 and 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Responsive to communication application 10/625,505 filed on 07/22/2003 and Applicant Amended filed on 03/09/2006, claims 1, 3-8, 11, 16, 20-23, 25, 27-28, 30-32, and 34-40 are pending.

Claims 1, 4, 8, 11, 16, 22, 30-32, and 35 have been amended.

Claims 2, 9-10, 12-15, 17-19, 24, 26, 29, and 33 have been canceled.

2.   Applicant's arguments with respect to claims 1, 3-8, 11, 16, 20-23, 25, 27-28, 30-32, and 34-40 have been considered but are moot in view of the new ground of rejection and the allowable subject matters in the last office action have been withdrawn.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 1, 4-8, 11, 16, 22, 32, 35-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Application Specification does not describe or define as the following limitations in the claims language:

As per claims 1, 4, 8, 11, 16, 22, 30, 32, 35 and 40, recited such the limitations "set of input parameters" and "output metric".

As per claims 5 and 36, recited "<u>random fluctuation</u>".

As per claim 6 and 37, recited "<u>random seed</u>".

As per claims 7 and 38, recited "<u>effort level</u>".

As per claims 8 and 39, recited "<u>a default cost of a given resource for placement</u>; <u>a default soft-limit for fitting or synthesis</u>; and <u>a coefficient indicating the speed versus source usage optimization for the compilation</u>".

As per claim 11, recited "<u>defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled</u>; <u>is a balancing parameter to technology mapping in synthesis</u>; <u>adds or deletes one optimization algorithm or step from a default CAD flow, or modifies an order-in which CAD steps are applied to the integrated circuit</u>; <u>is a choice or specification of an alternate synthesis optimization script</u>; <u>or enables a netlist optimization or physical resynthesis step</u>".

As per claim 40, recited "tuning parameter and exogenous" does not clearly describe in the specification what is the meaning and the functionality of "tuning parameter and exogenous". However, the word "exogenous" is defined the generic meaning by the dictionary, but without the functional and structure have been described.

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

6.   Claims 1, 3-8, 11, 16, 20-23, 25, 27-28, 30-32, and 34-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 4, 8, 11, 16, 22, 30, 32, 35 and 40, recited such the limitations "set of input parameters" and "output metric" are not point out and distinctly claim subject matter of what are particularly of "set of input parameter" and "output metric" that using in the invention?

As per claims 5 and 36, what is a particular of "the input parameters from random fluctuation"?

As per claim 6 and 37, what is a particular of "the input parameter is a random seed"?

As per claims 7 and 38, what is a particular of "the input parameter is effort level for the compilation tool"?

As per claims 8 and 39, what are a particular of the input parameter modifying of "a default cost of a given resource for placement; a default soft-limit for fitting or synthesis; and a coefficient indicating the speed versus source usage optimization for the compilation"?

As per claim 11, what is a particular of the input parameters of: defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled; is a balancing parameter to technology mapping in synthesis; adds or deletes one optimization algorithm or step from a default CAD flow, or modifies an order-in which CAD steps are applied to the integrated circuit; is a choice or specification of an alternate synthesis optimization script; or enables a netlist optimization or physical resynthesis step.

As per claim 40, recited "tuning parameter and exogenous" is not clearly described in the application specification and the claim language.

7.   Regarding claim 35, the phrase "<u>a metric of average results across a range</u> of input parameter" renders the claim indefinite because it is unclear whether the limitation(s) "<u>average results across a range</u>" the phrase are part of the claimed invention. See MPEP § 2173.05(d).

8.   As per claims 3, 20-21, 23, 25, 27-28, 31, and 34, are also rejected under 35 USC 112 first and second paragraphs, because these claims depend directly or indirectly from the forth set of claims which are containing unclear or undefined subject matter.

Claim Rejections - 35 USC § 101

9.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10.   The claims 1, 3-8, 11, 16, 20-23, 25, 27-28, 30-32, and 34-40 claimed invention is directed to non-statutory subject matter. Taking the claim 1 for exemplary that the invention claimed a method for compiling a design for an integrated circuit associated with a set of input parameters to generate an output metric and the compilation stops when criteria has been reached. Moreover, the method produces a table of result from the output metric with combination of the set of input parameters. In the combination of all the limitation of claim 1 and as similar to other independent claims, the claims language disclose an abstract idea of a conventional computer program compiler, they do not disclose any new, useful, or purpose of using the result from the invention. In the

conventional compilation, the compiler must have to have inputs to produce output and

may formatting the output in suitable format as a table associated with the inputs.

Claim Rejections - 35 USC § 102

11.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12.   Claims 1, 3-8, 11, 16, 20-23, 25, 27-28, 30-32, and 34-40 are rejected under 35

U.S.C. 102(b) as being anticipated by Karchmer et al. (Karchmer) (Sweeper.tcl, Version

2.3 Beta 05/02/2003).

13.   With respect to claims 1, 4, 8, 11, 16, 22, 32, and 35, Karchmer discloses a

method and computer system for compiling a design for an integrated circuit, the

method comprising:

(claims 1, 4, 8, 11, 16, 22, 32, and 35) automatically performing multiple

compilations of the design *(proc get_delay, proc get_period, proc get_all_clock_period,*

proc analyze_resource, proc analyze_and_store_result, proc do_compile, proc stop-

compiler, proc open_project, proc do_iteration, proc recover_from_backup, proc

run_sweep are running on Main program) (pages 7-27) using a series of values for each

input parameter in a set of input parameters *(enter seeds such as best_period,*

best_seed, best_slack, ..etc) (pages 7-27, proc get_delay, proc get_period, and proc

get_all_clock_period, page 16, puts "Compiling...." FITTING, TIMING ANALYSIS,

ASSEMBLER, NETLIST WRITER, page 25, Enter Seeds) to generate output values for

one or more output metrics *(output file or log file or open_project) (page 7-27, proc open_project, proc do_iteration, proc analyze_and_store_result, and proc recover_from_backup)*;

(claims 1, 4, 8, 11, 16, 22, 32, and 35) reporting the output values for the output metrics *(output file or log file or sweep_result.txt.) (page 14, proc analyze_and_store_result, page 17, proc open_project, pages 18-19, proc do_iteration, page 23, show status and display log, page 25, list all Tco and Tsu constraint option)* ; and

(claims 1, 4, 8, 11, 16, 22, 32, and 35) concluding the compilations when a stopping criteria has been reached *(page 16-17, proc stop-compiler, pages 26-27, Run and Stop bottoms)*,

(claims 1 and 32) wherein the method produces a table of results *(log-box, display log, -- setup table with frame, border width, set grid, ..etc.)* of the output metric for each combination of input parameter for a compilation *(pages 23-27, Main)*.

(claims 4 and 35) wherein the method produces a metric of average across a range of input parameter to indicate expected noise or variability *(see page 3, the average variance from the worst seed to best was approximately 7 percent)*.

(claim 8) wherein one of the input parameters modifies at least one-of: a default cost of a given resource for placement. a default soft-limit for fitting or synthesis, and a coefficient indicating the speed versus resource usage optimization for the compilations *(pages 3-4, introduction)*.

(claim 11) wherein at least one of the input parameters: defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled; is a balancing parameter to technology mapping in synthesis; adds or deletes one optimization algorithm or step from a default CAD flow or modifies an order in which CAD steps are applied to the integrated circuit is a choice or specification of an alternate synthesis optimization script; or enables a netlist optimization or physical resynthesis step *(pages 7-13 proc get_delay, proc get_period, proc get_all_clock_period)*.

(claims 16) wherein the output metrics include at least one of: a measure of the longest delay path in the design a quantification of logic area or other resource usage of the integrated circuit: an estimate of power consumption: and a metric for a number of paths, register-register pairs, IO-register pairs, or register-IO pairs that fail to meet a specified timing constraint *(pages 7-8, check slack if available, which get timing node (pin) and get timing node of register)*.

(claims 22) wherein the stopping criteria for the method is based on at least one of: exhausting all possible combination of specified input parameters independent of results: a total compile time consumed over all of the compilations thus far; the number of failing timing paths in the circuit; and a statistical calculation of possible success by the method *(page 5, stop compiler, best seed, and worst seed; and page 17)*.

14.   With respect to claims 3 and 34, Karchmer discloses all the limitation of the forth set of claims, wherein the method produces a signature of the best configuration of

input parameters, for use in future compilations *(page 4, Best seed based on, to save the best compile in the backup file)*.

15.   With respect to claims 5-7 and 36-39, Karchmer discloses all the limitation of the forth set of claims:

(claims 5 and 36) wherein the metric is used to distinguish gains due to the input parameters from random fluctuation.

(claims 6 and 37) wherein one of the input parameters is a random seed or initial configuration parameter *(page 2, change it to effect the initial placement configuration setting)*.

(claims 7 and 38) wherein one of the input parameters is effort level for the compilation tool or a portion of the compilation tool *(proc get_delay, proc get_period, proc get_all_clock_period, proc analyze_resource, proc analyze_and_store_result, proc do_compile, proc stop-compiler, proc open_project, proc do_iteration, proc recover_from_backup, proc run_sweep are running on Main program) (page 7-27)*

(Claim 39) wherein one of the input parameters modifies a default cost of a given resource for placement *(page 4, and page 13, proc analyze_resource)*.

16.   With respect to claims 20 and 21, Karchmer discloses all the limitation of the forth set of claims,

(Claim 20) wherein the set of output metrics includes a minimum slack *(best slack)* calculated on the integrated circuit design *(pages 13-16, proc analyze_resource, proc analyze_and_store_result)*.

(Claim 21) wherein the set of output metrics includes a total slack calculated on the integrated circuit design *(pages 13-16, proc analyze_resource, proc analyze-_and_store_result)*.

17.   With respect to claims 23, 25, and 27-28, Karchmer discloses all the limitation of the forth set of claims,

(Claim 23) wherein the stopping criteria is based on achieving a user's specified constraints *(page 4, Best Seed Based on)*.

(Claim 25) wherein the stopping criteria is based on a number of failed constraints in the integrated circuit *(page 4, Best Seed Based on)*.

(claim 27) wherein the stopping criteria is based on achieving a minimum worst-case slack in the integrated circuit *(page 4, Best Seed Based on)*.

(claim 28) wherein the stopping criteria is based on a total slack in the circuit *(page 4, Best Seed Based on and page 14)*.

18.   With respect to claim 30 and 31, Karchmer discloses all the limitation of the forth set of claims,

(claim 30) wherein automatically performing multiple compilations includes using a static schedule pre-calculated by a tool to select the series of values for each input parameter to be used in the compilations *(enter the seed for compiler)(pages 3-4, and parameter from the subroutine of program, pages 7-17)*

(claim 31) wherein the static schedule is dynamically modified based on a metric of current distance from the user goals *(time compilation) (pages 3 and 4)*.

19. With respect to claim 40, Karchmer discloses a method for determining tuning parameters for a CAD algorithm or tool, the method comprising: performing multiple compilations of a design of an integrated circuit *(proc get_delay, proc get_period, proc get_all_clock_period, proc analyze_resource, proc analyze_and_store_result, proc do_compile, proc stop-compiler, proc open_project, proc do_iteration, proc recover_from_backup, proc run_sweep are running on Main program) (pages 7-27)* using a series of values for each tuning parameter in a set of tuning parameters *(enter seeds such as best_period, best_seed, best_slack, ..etc) (pages 7-27, proc get_delay, proc get_period, and proc get_all_clock_period, page 16, puts "Compiling...." FITTING, TIMING ANALYSIS, ASSEMBLER, NETLIST WRITER, page 25, Enter Seeds)*; performing multiple compilations of the design using a series of exogenous parameters *(global slack) (enter seeds such as best_period, best_seed, best_slack, ..etc) (pages 7-27, proc get_delay, proc get_period, and proc get_all_clock_period, page 16, puts "Compiling...." FITTING, TIMING ANALYSIS, ASSEMBLER, NETLIST WRITER, page 25, Enter Seeds)*; generating outputs values for one or more output metrics *(output file or log file or sweep_result.txt.) (page 14, proc analyze_and_store_result, page 17, proc open_project, pages 18-19, proc do_iteration, page 23, show status and display log, page 25, list all Tco and Tsu constraint option)*; reporting the output values of the output metrics *(output file or log file or sweep_result.txt.) (page 14, proc analyze_and_store_result, page 17, proc open_project, pages 18-19, proc do_iteration, page 23, show status and display log, page 25, list all Tco and Tsu constraint option)*; and concluding efficacy of the tuning parameters in the presence of exogenous noise

(global slack) page 14, proc analyze_and_store_result, page 17, proc open_project, pages 18-19, proc do_iteration, page 23, show status and display log, page 25, list all Tco and Tsu constraint option).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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